

# Selecting the Best Serial EEPROM Interface Protocol for your Application

## 1. Introduction

- Atmel offers Serial Electrically Erasable Programmable Read Only Memories (SEEPROM) to designers wanting to save Printed Circuit Board Assembly (PCBA) area and simplify hardware design. Serial refers to the hardware interface scheme to write and read data from the device (two, three, or four signals needed). The parallel interface scheme to write and read data involves 18 or more signals. SEEPROM devices are 8 pin packages compared to 20 or more pins on parallel interface EEPROM devices. Since SEEPROMs have a smaller pin count than parallel EEPROMs, the SEEPROM device packages are smaller and therefore save PCBA area that would be consumed by the physically larger parallel EEPROM devices. Since SEEPROMs have a smaller pin count on device packages than parallel EEPROMs, there are fewer signals to route in the PCBA design.
- When an SEEPROM solution is desired, more decisions are needed to direct the designer to the best device for the application. The interface protocol decision is quite often driven by hardware and software features of the microcontroller that is to be interfaced to the SEEPROM. Atmel offers three protocol families of SEEPROMs:
  1. 2-Wire Interface (**TWI**) in the AT24CXXXX family [compatible with **I2C** protocol]
  2. 3-Wire Interface (**3WI**) in the AT93CXXX family
  3. Serial Peripheral Interface (**SPI**) in the AT25XXXX family
- The following device features will be discussed should the designer have the freedom to choose the interface protocol:
  - Interface signals
  - Chip Selection signal
  - Memory expansion
  - Maximum interface clock speeds
  - Command complexity
  - Write protection / data security
  - Cost

### 1.1. Interface Signals

- TWI:** a clock signal and a bi-directional data signal (SCL, SDA)
- 3WI:** a clock signal, a data in signal, and a data out signal (SK, DI, DO) [Chip Select is needed also]
- SPI:** a chip select signal, a clock signal, a data in signal, and a data out signal (CS, SCK, SI, SO)

**TWI fewest, 3WI and SPI have the same**



## Serial EEPROM Interface Protocol

## Application Note





## 1.2. Chip Select Function

- TWI:** has no chip select (CS) signal, always listening for commands
- 3WI:** CS is active high; CS must be high for device to listen for commands
- SPI:** CS is active low; CS must be low for device to listen for commands
- TWI does not need it, 3WI and SPI both have CS**

## 1.3. Memory Expansion

- TWI:** slave addressing supported (cascading), maximum 8 devices dependent upon device memory size
- 3WI:** utilizing independent chip selects, the SK, DI, and DO signals of multiple devices can be bussed
- SPI:** utilizing independent chip selects, the SCK, SI, and SO signals of multiple devices can be bussed
- TWI supports cascading, 3WI and SPI support bussing**

## 1.4. Maximum Interface Clock Speed

- TWI:** 1MHz
- 3WI:** 2MHz
- SPI:** 20MHz
- SPI fastest, 3WI next, TWI is slowest**

## 1.5. Command Complexity

- TWI:**
- Write Operation:
    - Send Start bit
    - Send device address byte with write bit embedded
    - Send word address byte
    - Send data byte(s) for byte write or page write
    - Send Stop bit to start write cycle
  - Read Operation:
    - Send Start bit
    - Send device address byte with write bit embedded (dummy write sequence)
    - Send device word address
    - Send device address byte with read bit embedded
    - Receive data byte(s)
    - Send Stop bit
- 3WI:**
- Write Operation:
    - Enable device via chip select high
    - Send write enable op code
    - Disable device via chip select low
    - Enable device via chip select high
    - Send write op code with address
    - Send data byte/word
    - Write cycle begins
    - Disable device via chip select low

Read Operation:  
Enable device via chip select high  
Send read op code with address  
Receive data byte(s)  
Disable device via chip select low

**SPI:** Write Operation:  
Enable device via chip select low  
Send write enable op code  
Disable device via chip select high  
Enable device via chip select low  
Send write op code with address  
Send data byte(s) for byte write or page write  
Disable device via chip select high to start write cycle

Read Operation:  
Enable device via chip select low  
Send read op code with address  
Receive data byte(s)  
Disable device via chip select high

**TWI command syntax is the simplest and supports byte and page writes.**

**3WI command syntax is more complex than TWI but 3WI only supports byte/word modes.**

**SPI command syntax is more complex than TWI and supports both byte and page writes.**

## 1.6. Write Protection / Data Security

**TWI:** Write Protect (WP) signal (active high) driven high: all, half, or a quarter of the memory array can be protected dependent upon device features

**3WI:** Write Enable op code, Write Disable op code

**SPI:** WP signal (active low) driven low: the memory array can not be written into when status register has WPEN bit set to "1"  
WP signal (active low) driven high: the memory array can be written into if status register has WPEN bit set to "0"  
Status register bits can be set on command to select none, a quarter, a half, or all of the memory array to be protected  
Since the device counts the serial clocks groups of eight, clock count mismatches cause commands to be aborted.

**TWI has hardware write protection data security only**

**3WI has software write protection data security only**

**SPI has hardware write protection data security that be overridden under software control and**

**SPI has better protocol checking by counting clocks**

## 1.7. Cost

**TWI:** Lowest expense  
**3WI:** Low expense  
**SPI:** Medium expense





## 2. Conclusion

- Choose TWI if:
  1. You have only two port signals available from the microcontroller
  2. You like the simpler commands
  3. You don't need the fastest clock speed
  4. You don't need to software override of the hardware write protection feature
  5. You need the highest density memory arrays
- Choose 3WI if:
  1. You have four port signals available from the microcontroller
  2. You can use the more complex, two step writing commands
  3. You like the medium speed interface
  4. You don't need hardware write protection
  5. You need the medium density memory arrays
- Choose SPI if:
  1. You have four port signals available from the microcontroller
  2. You like the counted clock protocol verification security
  3. You need the fastest clock speed interface
  4. You like the software override of the hardware write protection
  5. You need the highest density memory arrays

## 3. Revision History

*Table 1.* Revision History

| Doc. Rev. | Date    | Comments                  |
|-----------|---------|---------------------------|
| 8546A     | 06/2008 | Initial document release. |



---

## Headquarters

### **Atmel Corporation**

2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

---

## International

### **Atmel Asia**

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### **Atmel Europe**

Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

### **Atmel Japan**

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

---

## Product Contact

### **Web Site**

[www.atmel.com](http://www.atmel.com)

### **Technical Support**

[s\\_eeeprom@atmel.com](mailto:s_eeeprom@atmel.com)

### **Sales Contact**

[www.atmel.com/contacts](http://www.atmel.com/contacts)

### **Literature Requests**

[www.atmel.com/literature](http://www.atmel.com/literature)

---

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2008 Atmel Corporation. All rights reserved. Atmel®, logo and combinations thereof, and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.