# High-Speed Analog Comparator with Slope Compensation DAC

## HIGHLIGHTS

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**Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device, this manual section may not apply to all dsPIC33/PIC24 devices. Some dsPIC33/PIC24 devices are dual core and contain both a Primary and Secondary CPU core. For single core dsPIC33/PIC24 devices, disregard any Secondary-specific references.

Please consult the note at the beginning of the **"High-Speed Analog Comparator with Slope Compensation DAC"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Website at: http://www.microchip.com.

## 1.0 INTRODUCTION

The High-Speed Analog Comparator with Slope Compensation DAC module provides a way to monitor voltage, current and other critical signals in a power conversion application that may be too fast for the CPU and ADC to capture. Each High-Speed Analog Comparator module is comprised of a high-speed comparator, Pulse Density Modulation (PDM) DAC and a slope compensation unit.

The number of instances of the DAC/comparator modules is device-dependent. Refer to the device-specific data sheet for availability. The comparator module can be used to implement Peak Current-mode control, Critical Conduction mode and hysteretic control-based power supplies.

The High-Speed Analog Comparator with Slope Compensation DAC consists of the following key features:

- Rail-to-Rail Analog Comparator
- Up to Five Selectable Input Sources per Comparator:
  - Up to four external inputs
  - Up to three internal inputs from the PGA module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Interrupt Generation Capability
- Dedicated Pulse Density Modulation (PDM) Digital-to-Analog Converter (DAC) for Each Analog Comparator:
  - 12-bit resolution
- Multimode Multipole RC Output Filter:
  - Transition mode: Provides the fastest response
  - Fast mode: For tracking DAC slopes
  - Steady-State mode: Provides 12-bit resolution
- Dedicated Support for the Following Modes:
  - Slope Generation
  - Hysteretic Control
  - Triangle Wave
- Functional Support for the High-Speed PWM Module which Includes:
  - PWM duty cycle control
  - PWM period control
  - PWM Fault detect

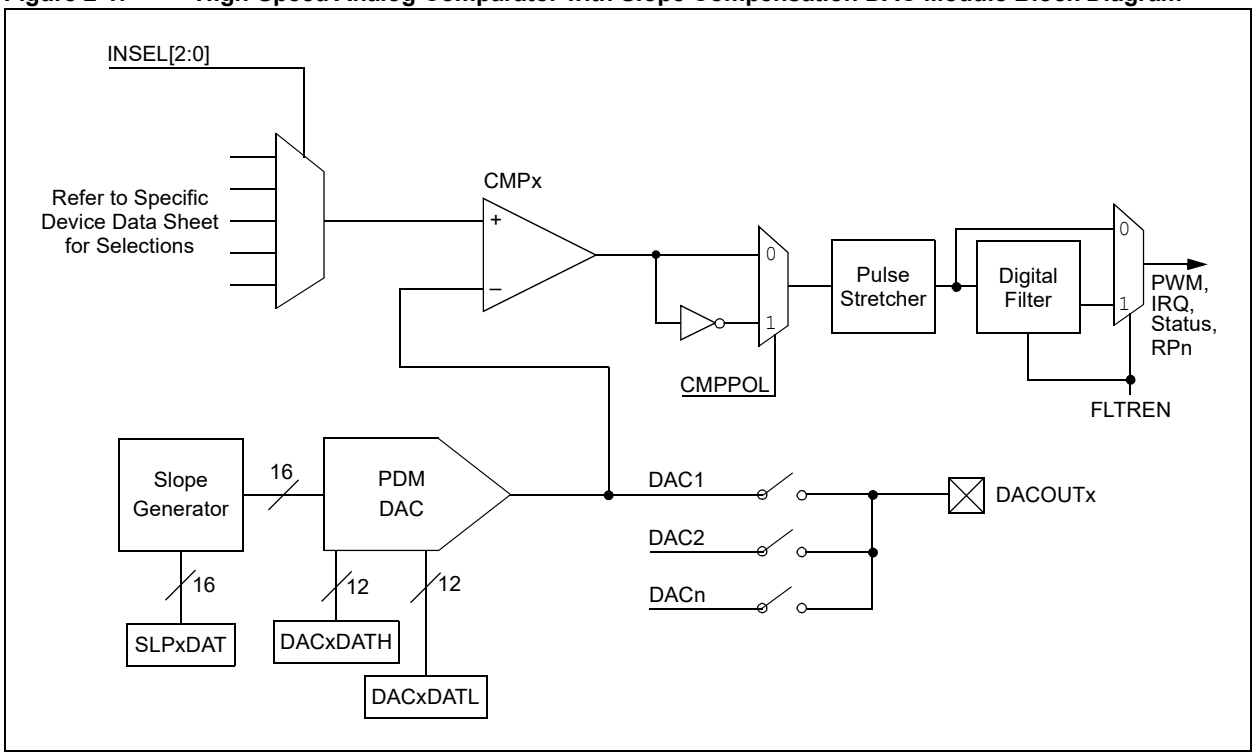
## 2.0 MODULE DESCRIPTION

The High-Speed Analog Comparator with Slope Compensation DAC module is comprised of a high-speed comparator, Pulse Density Modulation (PDM) DAC and a slope compensation unit. Devices typically have multiple instances of the module. Refer to the specific device data sheet for the number of available modules.

The slope compensation unit provides a user-defined slope which can be used to alter the DAC output. This feature is useful in applications, such as Peak Current-mode control, where slope compensation is required to maintain the stability of the power supply. The user specifies the direction and rate of change for the slope compensation, and the output of the DAC is modified accordingly. The DAC consists of a PDM unit, followed by a digitally controlled multistage RC filter. The PDM unit uses a phase accumulator circuit to generate an output stream of pulses. The density of the pulse stream is proportional to the input data value, relative to the maximum value supported by the bit width of the accumulator. The output pulse density is representative of the desired output voltage. The pulse stream is filtered with an RC filter to yield an analog voltage. The output of the DAC is connected to the negative input of the comparator. The positive input of the comparator can be selected using a MUX from either the input pins or the output of the PGAs. The comparator provides a high-speed operation with a typical delay of 15 ns. The output of the comparator can be processed by pulse stretcher and digital filter blocks, which prevent comparator response to unintended fast transient signals.

Figure 2-1 shows a block diagram of the High-Speed Analog Comparator with Slope Compensation DAC module. The DAC module can be operated in one of four modes: Slope Generation, Triangular Wave, Hysteretic or as a normal 12-bit DAC. Each of these modes can be used in a variety of power supply applications, such as Peak Current-mode control, Critical Conduction mode control and Hysteretic Control mode.

**Figure 2-1: High-Speed Analog Comparator with Slope Compensation DAC Module Block Diagram**



# 3.0 CONTROL REGISTERS

There are two classes of control registers for the comparator/DAC modules: common and instance-specific.The registers, DACCTRL1 and DACCTRL2, specify common configuration settings for the DAC modules. All of the other registers specify settings exclusively for the individual DAC instance ‘x’. Devices that support both Primary and Secondary cores have complete and separate sets of control registers.

**Note:** x = Refer to the specific device data sheet for the available Primary and Secondary modules.

## 3.1 Register Map

A summary of the registers associated with the High-Speed Analog Comparator with Slope Compensation DAC is provided in Table 3-1.

**Table 3-1: High-Speed Analog Comparator Registers**

| File Name | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DACCTRL1L | DACON | — | DACSIDL | — | — | — | — | — | CLKSEL[1:0] | | CLKDIV[1:0] | | — | FCLKDIV[2:0] | | |
| DACCTRL2H | — | — | — | — | — | — | SSTIME[9:0] | | | | | | | | | |
| DACCTRL2L | — | — | — | — | — | — | TMODTIME[9:0] | | | | | | | | | |
| DACxCONH | — | — | — | — | — | — | TMCB[9:0] | | | | | | | | | |
| DACxCONL | DACEN | IRQM[1:0] | | — | — | CBE | DACOEN | FLTREN | CMPSTAT | CMPPOL | INSEL[2:0] | | | HYSPOL | HYSSEL[1:0] | |
| DACxDATH | — | — | — | — | DACDAT[11:0] | | | | | | | | | | | |
| DACxDATL | — | — | — | — | DACLOW[11:0] | | | | | | | | | | | |
| SLPxCONH | SLOPEN | — | — | — | HME | TWME | PSE | — | — | — | — | — | — | — | — | — |
| SLPxCONL | HCFSEL[3:0] | | | | SLPSTOPA[3:0] | | | | SLPSTOPB[3:0] | | | | SLPSTRT[3:0] | | | |
| SLPxDAT | SLPDAT[15:0] | | | | | | | | | | | | | | | |

**Legend:** — = unimplemented bit, read as ‘0’; x = number of available comparator/DAC modules.

**Register 3-1: DACCTRL1L: DAC Control 1 Low Register**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DACON | — | DACSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CLKSEL[1:0](1) | | CLKDIV[1:0](1) | | — | FCLKDIV[2:0](2) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15 **DACON:** Common DAC Module Enable bit
1 = Enables DAC modules
0 = Disables DAC modules

bit 14 **Unimplemented:** Read as '0'

bit 13 **DACSIDL:** DAC Stop in Idle mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7-6 **CLKSEL[1:0]:** DAC Clock Source Select bits(1)
Refer to device-specific data sheet for selections.

bit 5-4 **CLKDIV[1:0]:** Clock Divider bits(1)
11 = Divide by 4
10 = Divide by 3 (non-uniform duty cycle)
01 = Divide by 2
00 = 1x

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **FCLKDIV[2:0]:** Comparator Filter Clock Divider bits(2)
111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = 1x

**Note 1:** These bits should only be changed when DACON = 0 to avoid unpredictable behavior.
**2:** The input clock to this divider is the selected clock input, CLKSEL[1:0], and then divided by two.

**Register 3-2: DACCTRL2H: DAC Control 2 High Register**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | SSTIME[9:8](1,2) | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSTIME[7:0](1,2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SSTIME[9:0]:** Transition Start Mode until Steady-State Filter is Enabled bits(1,2)

**Note 1:** The value for SSTIME[9:0] should be greater than the TMODTIME[9:0] bits.

**2:** Default value for SSTIME[9:0] = 0x8A.

**Register 3-3: DACCTRL2L: DAC Control 2 Low Register**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | TMODTIME[9:8](1,2) | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| TMODTIME[7:0](1,2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **TMODTIME[9:0]:** Duration of Transition Mode bits(1,2)

**Note 1:** The value for TMODTIME[9:0] should be less than the SSTIME[9:0] bits.

**2:** Default value for TMODTIME[9:0] = 0x55.

**Register 3-4: DACxCONH: DACx Control High Register**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | TMCB[9:8] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TMCB[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **TMCB[9:0]:** DACx Leading-Edge Blanking bits

This register specifies the blanking period in counts of 2/FDAC for the comparator, following changes to the DACx output during Change-of-State (COS) for the input signal selected by the HCFSEL[3:0] bits in Register 3-9.

**Register 3-5: DACxCONL: DACx Control Low Register**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DACEN | IRQM[1:0](1,2) | | — | — | CBE | DACOEN | FLTREN |
| bit 15 | | | | | | | bit 8 |

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CMPSTAT | CMPPOL | INSEL[2:0] | | | HYSPOL | HYSSEL[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15 **DACEN:** Individual DACx Module Enable bit
1 = Enables DACx module
0 = Disables DACx module and disables FSCM clock to reduce power consumption; any pending Slope mode and/or underflow conditions are cleared

bit 14-13 **IRQM[1:0]:** Interrupt Mode Select bits(1,2)
11 = Generates an interrupt on either a rising or falling edge detect
10 = Generates an interrupt on a falling edge detect
01 = Generates an interrupt on a rising edge detect
00 = Interrupts are disabled

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CBE:** Comparator Blank Enable bit
1 = Enables the analog comparator output to be blanked (gated off) during the recovery transition, following the completion of a slope operation
0 = Disables the blanking signal to the analog comparator; therefore, the analog comparator output is always active

bit 9 **DACOEN:** DACx Output Buffer Enable bit
1 = DACx analog voltage is connected to the DACOUTx pin
0 = DACx analog voltage is not connected to the DACOUTx pin

bit 8 **FLTREN:** Comparator Digital Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 7 **CMPSTAT:** Comparator Status bit
Current state of the comparator output including the CMPPOL selection.

bit 6 **CMPPOL:** Comparator Output Polarity Control bit
1 = Output is inverted
0 = Output is noninverted

bit 5-3 **INSEL[2:0]:** Comparator Input Source Select bits
See device-specific data sheet for selections.

bit 2 **HYSPOL:** Comparator Hysteresis Polarity Select bit
1 = Hysteresis is applied to the falling edge of the comparator output
0 = Hysteresis is applied to the rising edge of the comparator output

bit 1-0 **HYSSEL[1:0]:** Comparator Hysteresis Select bits
11 = 45 mV hysteresis
10 = 30 mV hysteresis
01 = 15 mV hysteresis
00 = No hysteresis is selected

**Note 1:** Changing these bits during operation may generate a spurious interrupt.
**2:** The edge selection is a post-polarity selection via the CMPPOL bit.

**Register 3-6: DACxDATH: DACx Data High Register**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | DACDAT[11:8](1) | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DACDAT[7:0](1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **DACDAT[11:0]:** DACx Data bits(1)

This register specifies the high DACx data value, $V_{DAC}$ = DACDAT * ($V_{DD}$)/4095.
Valid values are from 205 (0x0CD) to 3890 (0xF32).
111100110011 to 111111111111 = Reserved
111100110010 = 0.95 * $V_{DD}$
•
•
11001101 = 0.05 * $V_{DD}$
000000000000 to 11001100 = Reserved

**Note 1:** When operating in Slope mode or Triangle Wave mode, the DACDAT value must be greater or equal to (5 x SLPDAT) + DACLOW.

**Register 3-7: DACxDATL: DACx Data Low Register**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | DACLOW[11:8](1) | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DACLOW[7:0](1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **DACLOW[11:0]:** DACx Low Data bits(1)

In Hysteretic mode, Slope Generator mode and Triangle mode, this register specifies the low data value and/or limit for the DACx module. VOUT = DACDAT * (VDD)/4095. Valid values are from 205 (0x0CD) to 3890 (0xF32).

111100110011 to 111111111111 = Reserved
111100110010 = 0.95 * VDD
•
•
11001101 = 0.05 * VDD
000000000000 to 11001100 = Reserved

**Note 1:** When operating in Slope mode or Triangle Wave mode, the DACLOW value must be less than or equal to DACDAT – (5 x SLPDAT).

**Register 3-8: SLPxCONH: DACx Slope Control High Register**

| R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SLOPEN | — | — | — | HME(1) | TWME(2) | PSE | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15 **SLOPEN:** Slope Function Enable/On bit
1 = Enables slope function
0 = Disables slope function; slope accumulator is disabled to reduce power consumption

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **HME:** Hysteretic Mode Enable bit(1)
1 = Enables Hysteretic mode for DACx
0 = Disables Hysteretic mode for DACx

bit 10 **TWME:** Triangle Wave Mode Enable bit(2)
1 = Enables Triangle Wave mode for DACx
0 = Disables Triangle Wave mode for DACx

bit 9 **PSE:** Positive Slope Mode Enable bit
1 = Slope mode is positive (increasing)
0 = Slope mode is negative (decreasing)

bit 8-0 **Unimplemented:** Read as '0'

**Note 1:** HME mode requires the user to disable the slope function (SLOPEN = 0).
**2:** TWME mode requires the user to enable the slope function (SLOPEN = 1).

**Register 3-9: SLPxCONL: DACx Slope Control Low Register**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| HCFSEL[3:0] | | | | SLPSTOPA[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SLPSTOPB[3:0] | | | | SLPSTRT[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set0 | '0' = Bit is cleared |

bit 15-12 **HCFSEL[3:0]:** Hysteretic Comparator Function Input Select bits
The selected input signal controls the switching between the DACx high limit (DACxDATH) and the DACx low limit (DACxDATL) as the data source for the PDM DAC; it modifies the polarity of the comparator, and the rising and falling edges initiate the start of the LEB counter (TMCB[9:0] bits in Register 3-4). See the device-specific data sheet for assignments.

bit 11-8 **SLPSTOPA[3:0]:** Slope Stop A Signal Select bits
The selected Slope Stop A signal is logically ORed with the selected Slope Stop B signal to terminate the slope function. See the device-specific data sheet for assignments.

bit 7-4 **SLPSTOPB[3:0]:** Slope Stop B Signal Select bits
The selected Slope Stop B signal is logically ORed with the selected Slope Stop A signal to terminate the slope function. See the device-specific data sheet for assignments.

bit 3-0 **SLPSTRT[3:0]:** Slope Start Signal Select bits

**Register 3-10: SLPxDAT: DACx Slope Data Register(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SLPDAT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SLPDAT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 15-0 **SLPDAT[15:0]:** Slope Ramp Rate Value in 12.4 Format bits
This value represents the number of counts the DAC changes in a 2/FDAC step.

**Note 1:** Register data are left justified.

# 4.0 CONFIGURATION AND OPERATION

The High-Speed Analog Comparator with Slope Compensation DAC module is comprised of various blocks, such as a comparator, DAC, etc. The functionality and configuration of different blocks are discussed in this section.

## 4.1 Comparator Stage

### 4.1.1 COMPARATOR INPUTS

The inputs to the comparator module are configured using the DACxCONL register. Each comparator has up to five device-specific inputs, as shown in Figure 2-1. Refer to the device-specific data sheet for selections. The INSEL[2:0] bits (DACxCONL[5:3]) are used to select the comparator input source. The positive input of the comparator is connected to one of the selected input sources, while the negative input is always internally connected to the DAC output.

### 4.1.2 COMPARATOR OUTPUTS

The comparator output can be used to trigger PWM modules or interrupts for action based on the comparator event. When the digital filter is disabled, the comparator signal is made directly available to the PWM module as a current limit and/or Fault signal. This ensures minimal latency for Current-mode applications and for time-critical (safety) applications. The status signal and the interrupt request signal will be processed by the pulse stretcher circuit. When the digital filter is enabled, the PWM trigger signal, status signal and interrupt request signal are all processed by the pulse stretcher and the digital filter logic. This will cause a delay in the current limit/Fault limit event. The polarity of the comparator output is selected by configuring the CMPPOL bit (DACxCONL[6]). The comparator output can be monitored on the I/O pin by configuring the Peripheral Pin Select (PPS) register.

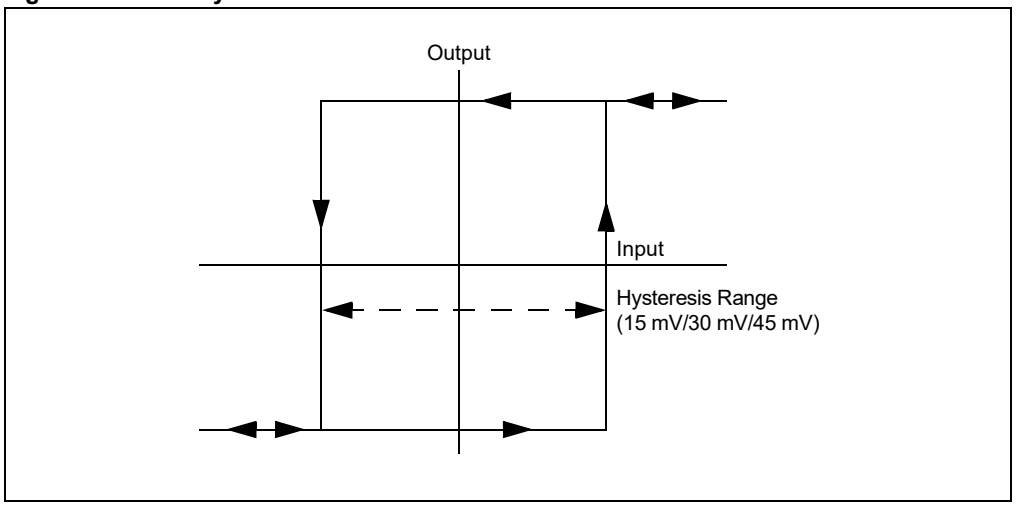
### 4.1.3 COMPARATOR INTERRUPT

The analog comparator interrupt can be used to service the comparator switching event and can be enabled or disabled from the interrupt controller. The analog comparator interrupt can be configured to interrupt on the rising edge, falling edge or both by setting the IRQM[1:0] bits (DACxCONL[14:13]). The comparator interrupt signal is generated on the selected edge of the comparator output, following the polarity processing through the CMPPOL bit (DACxCONL[6]), and the subsequent processing by the pulse stretcher and the digital filter logic. If the CMPPOL bit is changed during operation, the bit change will not cause an interrupt. Only the selected edge of an actual change of the comparator output status will initiate an interrupt.

### 4.1.4 COMPARATOR HYSTERESIS CONTROL

The HYSSEL[1:0] bits in the DACxCONL register specify the amount of hysteresis for the analog comparator. The HYSPOL bit specifies whether hysteresis is applied to the rising edge or falling edge of the signal. Configuration of hysteresis helps the comparator to avoid oscillation (i.e., toggling of the comparator output), which could be caused by noise on the positive input.

**Figure 4-1: Hysteresis Control**




### 4.1.5 PULSE STRETCHER

The High-Speed Analog Comparator can respond to very fast transient signals. To avoid a comparator malfunction, after choosing the comparator output polarity using the CMPPOL bit (DACxCONL[6]), the signal is passed to a pulse stretching circuit. The pulse stretching circuit waits for the comparator output to transition to a high state or a low state and then will stretch the signal for three clock cycles. For example, a comparator output signal of '01000101000' will be modified by the pulse stretcher circuit to '01110111110'. The pulse stretcher clock operates at a frequency of FDAC/2 and uses the DAC clock setting bits, CLKSELx and CLKDIVx. A configuration example to set the pulse stretcher is shown in Example 4-1.

**Example 4-1: Configuration for Pulse Stretcher**

```
/* Pulse Stretcher Configuration */
DAC1CONLbits.CMPPOL = 0;              /* Non inverted comparator output*/
DACCTRL1Lbits.CLKSEL = 2;             /* FDAC = AFPLL Auxillary PLL out */
DACCTRL1Lbits.CLKDIV = 1;             /* Divide by 2 */
```

### 4.1.6 DIGITAL FILTER

In many motor and power control applications, the analog comparator input signals can be corrupted by the large electromagnetic fields generated by the external switching power transistors. Corruption of the analog input signals to the comparator can cause unwanted comparator output transitions. A digital output filter can minimize the effects of the input signal corruption. The digital filter processes the comparator signal from the pulse stretcher circuit. The digital filter is enabled by the FLTREN bit (DACxCONL[8]). The digital filter operates with the clock selected by the CLKSEL[1:0] bits (DACCTRL1L[7:6]) and FCLKDIV[2:0] bits (DACCTRL1L[2:0]). The pulse stretcher output signal must be stable, either in a high state or a low state, for at least three times the selected filter clock frequency, for it to pass through the digital filter. Assuming the current state is '0', a comparator output string of '0011110000000000' gets modified by the pulse stretcher to '0011111100000000' and to '0000000001111110' by the digital filter if the filter clock frequency is divided by two. Because of the requirement of three similar consecutive states for the filter, the selected digital filter clock period must be one third or less than the maximum desired comparator response time. In Sleep mode or Idle mode, the digital filter is bypassed to enable an asynchronous signal from the comparator to the interrupt controller. This asynchronous signal can be used to wake-up the processor from Sleep mode or Idle mode. A configuration example to enable the digital filter is provided in Example 4-2.

**Example 4-2: Configuration for Digital Filter**

```
DACCTRL1Lbits.FCLKDIV = 1;  /* Filter Clk Divide by 2 */
DAC1CONLbits.FLTREN = 1;    /* Filter enabled */
```

## 4.2 Pulse Density Modulation (PDM) DAC

Each instance of the High-Speed Analog Comparator with Slope Compensation DAC has a dedicated DAC that is used to program the comparator threshold voltage via the DACxDATH register. The DAC comprises a digital Pulse Density Modulation (PDM) module, followed by a multistage RC filter. The PDM module generates a high-frequency output signal, whose density is proportional to the DACxDATH register value. The PDM module clock is selected by the CLKSEL[1:0] and CLKDIV[1:0] bits of the DACCTRL1L register. The clock selection plays an important role in the dynamic performance of the DAC module.

The DACxDATH register value has limits of 0x0CD and 0xF32, and will provide a DAC output of 5% to 95% of $V_{DD}$. For any intermediate value in the register, between 0xCD and 0xF32, the output voltage of the DAC will be proportional. The equation to calculate the DAC output voltage, based on the $V_{DD}$ voltage source, is provided in Equation 4-1 and Register 3-6. The DAC voltage can be varied in steps of $V_{DD}/(2^N - 1)$, where N is the number of DAC bits (N = 12). The DAC modules are controlled by the DACON bit (DACCTRL1L[15]). The DACON bit enables or disables all of the comparator modules instantiated on a given device or device core. The DACEN bit (DACxCONL[15]) provides individual control of the DAC module. The individual DAC registers have an output enable bit, DACOEN (DACxCONL[9]), which enables the DAC output voltage to be routed to an external output pin, DACOUTx. Some devices may have more than one DACOUTx pin. Typically, DAC instances 1-3 are assigned to DACOUT1, and DAC instances 4-6 are assigned to DACOUT2. Refer to the specific device data sheet for availability. The DACOUTx pin can only be associated with a single DAC or PGA output (if available on the device) at any given time. If more than one DACOEN bit is set, or the PGA Output Enable bit (PGAOEN) and the DACOEN bit are set, the DACOUTx pin will be a combination of the signals. A configuration example to set the DAC output voltage is shown in Example 4-3.

**Equation 4-1: DAC Output**

$$V_{DAC} = DACDAT \bullet (V_{DD})/4095$$

Where:
0x0CD ≤ DACDAT ≤ 0xF32

**Example 4-3: Configuration of DAC Register**

```
/* DAC Register Settings */
DAC1DATHbits.DACDATH = 0x4D9;      /* DAC Output set to 1V (VDD = 3.3V)*/
DAC1CONLbits.DACOEN = 1;           /* Enable DAC 1 output on pin DACOUT1 */
DAC1CONLbits.DACEN = 1;            /* Enable Master DAC 1 */
DACCTRL1Lbits.DACON = 1;           /* Turn ON all Master DACs */
```

### 4.2.1 SLOPE GENERATOR

The function of the slope generator is to vary the DAC data value at a user-defined rate to reach a desired endpoint value. The slope generator, along with the DAC, has three modes of operation; namely: Slope Generation mode, Hysteretic mode and Triangle Wave mode.

#### 4.2.1.1 Slope Generation Mode

The slope generator function can be utilized in Peak Current-mode control-based power supply applications, where slope compensation is required. The slope function modifies the non-slope PDM DAC value repeatedly, at a user-defined rate, until the DAC data value reaches its endpoint. The slope generation function can be enabled or disabled by the SLOPEN bit (SLPxCONH[15]). The slope rate is controlled by the data in the SLPxDAT register (Register 3-10). The direction of slope being positive or negative is controlled by the PSE bit (SLPxCONH[9]). For negative slopes (default, PSE = 0), the DACxDATH holds the nominal non-slope count, while the DACxDATL register holds the count corresponding to the end of the slope. For positive slopes (PSE = 1), the DACxDATL holds the nominal non-slope count, while the DACxDATH register holds the count corresponding to the end of the slope.

The slope generation start is controlled by the bits, SLPSTRT[3:0] (SLPxCONL[3:0]). Depending on the value of SLPSTRT[3:0], the selected PWM trigger will be used to start the slope generation. The DAC output voltage changes to the value in the DACxDATH register first by going to the Transition mode and then to the Steady-State mode. In Transition mode, the filter responds to new data values as fast as possible. The Transition mode duration is specified by the TMODTIME[9:0] bits (DACCTRL2L[9:0]). The source of the clock for the DAC operation is selected by bits, CLKSEL[1:0], and the frequency of operation ($F_{DAC}$) is set by the divider bits, CLKDIV[1:0] of the DACCTR1L register. The Transition mode duration, $T_{TR}$, is given by the equation:

**Equation 4-2:**

$$T_{TR} = TMODTIME[9:0] * 2/F_{DAC} \text{ in Seconds}$$

Where:
$F_{DAC}$ = DAC Frequency in Hz

The steady-state timer, specified by the SSTIME[9:0] bits, starts at the same time as the Transition mode timer. Once the Transition mode ends, the Steady-State mode starts, wherein the DAC output voltage settles to the new value. The Steady-State Time, $T_{SS}$, is calculated by the equation:

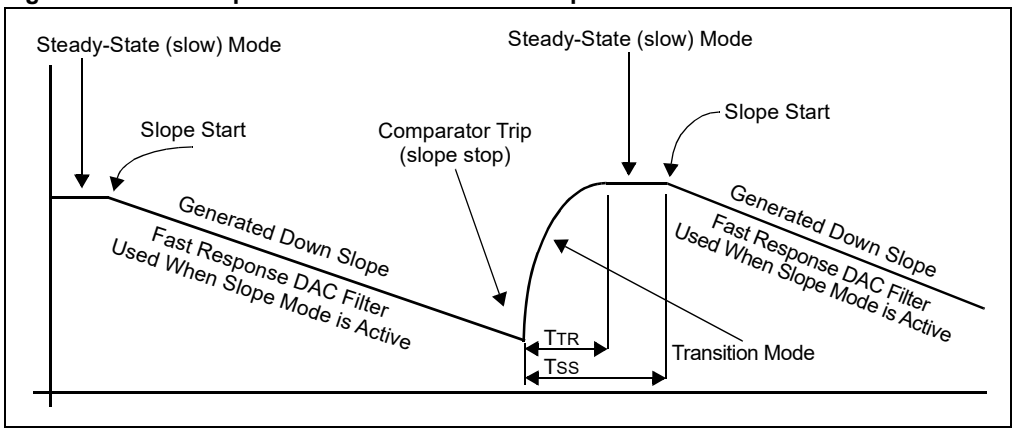
**Equation 4-3:**

$$T_{SS} = SSTIME[9:0] * 2/F_{DAC} \text{ in Seconds}$$

Note that the SSTIME[9:0] count should always be greater than the TMODTIME[9:0] count (Figure 4-2). At the end of the Steady-State mode, the DAC value settles at the new value and is ready for slope generation. The SLPSTRT[3:0] signal triggers the slope generation process.

Refer to the device-specific data sheet's DAC electrical specification for additional information on $T_{SS}$ and $T_{TR}$ values. These timing parameters can be additionally adjusted as needed for the application.

**Figure 4-2: Slope Generation Mode DAC Output Waveform**




The slope generation is terminated when one of the two stop signals is asserted. The eight control register bits, SLPSTOPA[3:0] (SLPxCONL[11:8]) and SLPSTOPB[3:0] (SLPxCONL[7:4]), select the control signal to terminate the slope generation. The stop signals are logically ORed so that the slope is terminated when one of the trigger events materializes. In most power supply applications, SLPSTOPA[3:0] can be configured to terminate the slope at the end of the PWM cycle, while SLPSTOPB[3:0] can be configured to trigger when the current reaches a limit under a normal or Fault condition. It should be noted that the stop signal must terminate the slope at the least TSS (Steady-State Time) prior to the next PWM cycle start. This is necessary to allow the DAC value to reach and settle at the steady-state value, specified by the DACxDATH register, before the next cycle begins.

The slope rate value to be specified in the SLPxDAT register depends on the start and end values of the slope specified by the DACxDATH and DACxDATL registers, PWM time period, DAC clock frequency and the SSTIME[9:0] bits value. The SLPxDAT value can be determined by using Equation 4-4. A configuration example to use Slope Compensation mode is shown in Example 5-1.

**Equation 4-4: Determining the SLPxDAT Value(1)**

$$SLPxDAT = \frac{(DACxDATH - DACxDATL) \bullet 16}{(T_{SLOPE\_DURATION})/T_{DAC}}$$

Where:

$DACxDATH$ = DAC value at the start of slope

$DACxDATL$ = DAC value at the end of slope

$T_{SLOPE\_DURATION}$ = Slope duration time in seconds

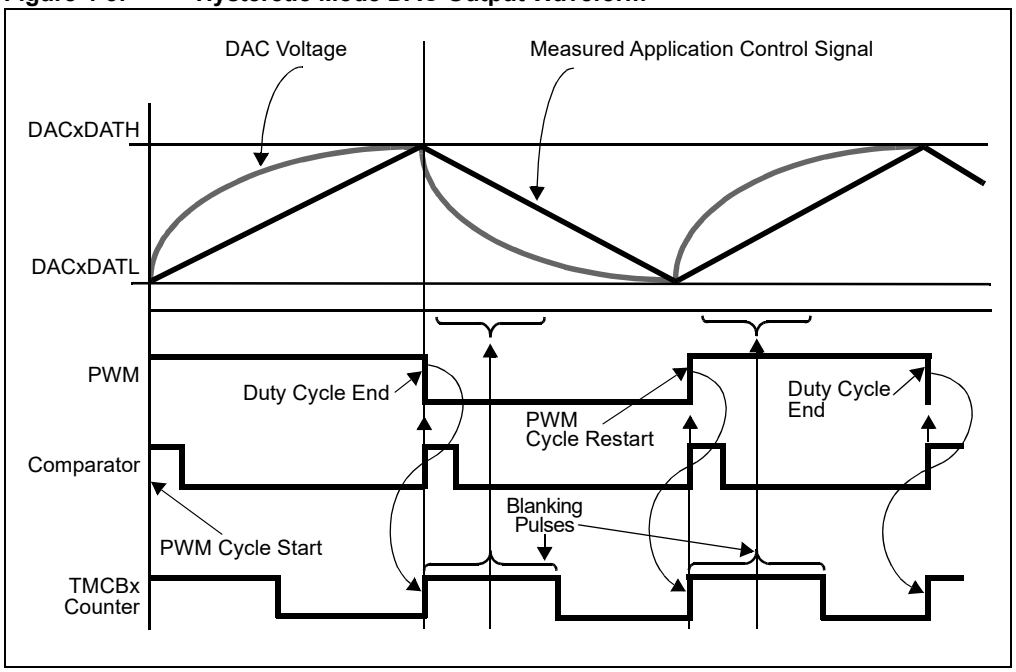
$T_{DAC}$ = 2/FDAC in seconds

**Note 1:** Multiplication by 16 sets the SLPxDAT value in 12.4 format.

#### 4.2.1.2 Hysteretic Mode

Hysteretic mode control is sometimes called “Bang-Bang” control, where a signal within a power converter is controlled within an upper cutoff and a lower cutoff limit. The Hysteretic mode is used in power supply applications utilizing hysteretic control, such as LED drivers. The Hysteretic mode is enabled by the HME bit (SLPxCONH[11]) and requires the SLOPEN bit to be cleared. Hysteretic Control mode enables a single DAC and comparator to monitor both the high and low limits for a signal. The DACxDATH register provides the higher value, while the DACxDATL register provides the lower value. When the DAC changes direction, the DAC uses Transition mode to respond and reach the new value as fast as possible. In Hysteretic mode, the comparator effectively functions as a window comparator. The DAC output races ahead of the monitored voltage in the application circuit. While the DAC is transitioning to the new value, the comparator output is “blanked” via the TMCB[9:0] bits (DACxCONH[9:0]) to prevent spurious responses. The state of the PWM output is monitored via the input multiplexer controlled by the HCFSEL[3:0] bits of the SLPxCONL register. This module monitors the actual state of the PWM output rather than make assumptions that could damage the application circuit. A configuration example to use Hysteretic mode is shown in Example 5-2.

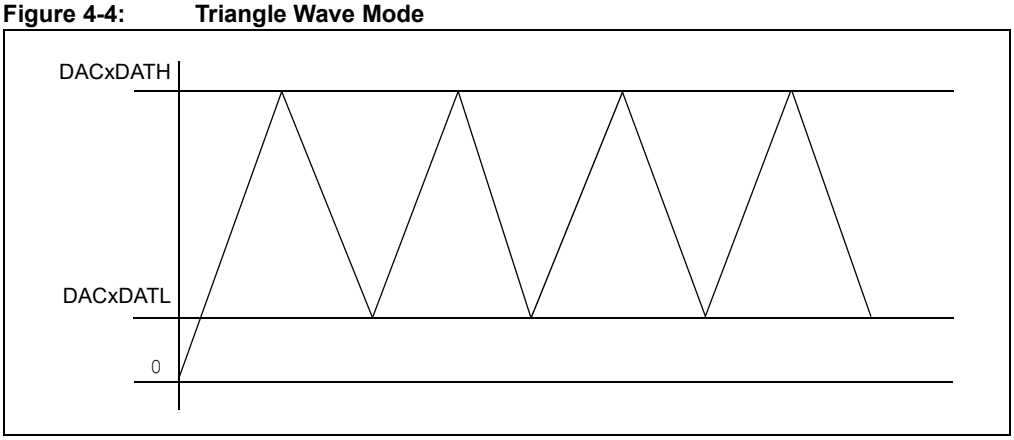
**Figure 4-3: Hysteretic Mode DAC Output Waveform**



#### 4.2.1.3 Triangle Wave Mode

Triangle Wave mode generates an output voltage that rises and falls with a triangle wave pattern. The Triangle Wave mode is enabled by the bit, TWME (SLPxCONH[10]), and requires SLOPEN to be set to '1'. The high and low points of the waveform are specified via the DACxDATH and DACxDATL registers. The rise and fall times, and the frequency of the triangle wave are controlled via the SLPxDAT register. The very first clock cycle of the slope process selects a scaled SLPxDAT value, instead of the specified value, to provide prompt DAC response to the DAC trajectory. For all subsequent clock cycles of the slope process, the slope generator uses the specified SLPxDAT data value for incrementing/decrementing the DAC data value. The Fast DAC mode is exclusive to the Triangle Wave mode and is used to provide a fast response. The slope changes the direction automatically after reaching either the DACxDATH or DACxDATL value. The Triangle Wave mode is useful in digital audio applications, where an analog input signal is sampled via an analog comparator using a triangle wave reference signal (Figure 4-4).

**Figure 4-4: Triangle Wave Mode**




A configuration example to set the Triangle Wave mode is shown in Example 4-4.

**Example 4-4: Triangle Wave Mode Configuration(1)**

```
/* Triangle Wave Mode Settings */
DAC1DATLbits.DACLOW = 0x100;      // Lower data value
DAC1DATHbits.DACDAT = 0xF00;      // Upper data value
SLP1DATbits.SLPDAT = 0x1;         // Slope rate, counts per step
SLP1CONHbits.TWME = 1;            // Enable Triangle Mode
SLP1CONHbits.SLOPEN = 1;          // Enable Slope mode
```

**Note 1:** The maximum value of DACxDATH must be set at 0xF32 – SLPxDAT and the minimum value of DACxDATL must be set at 0xCD + SLPxDAT.

## 4.3 Operation in Sleep and Idle Mode

During Sleep mode, the High-Speed Analog Comparator operates with reduced functionality, allowing the device to wake-up when an active signal is applied to the comparator input. To reduce power consumption when the device enters Idle mode, the comparator module can be disabled by setting the DACSIDL bit (DACCTRL1L[13]). The DACSIDL bit controls all the comparators on a device or device core.

# 5.0 APPLICATION INFORMATION

The High-Speed Analog Comparator with Slope Compensation DAC can be used in many power conversion applications. The outputs of the comparator module can be used to perform the following functions:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWM Signal (Current Limit)
- Truncate the PWM Period (Current Reset)
- Extend the PWM Period (Feed Forward)
- Disable the PWM Outputs (Fault Latch)

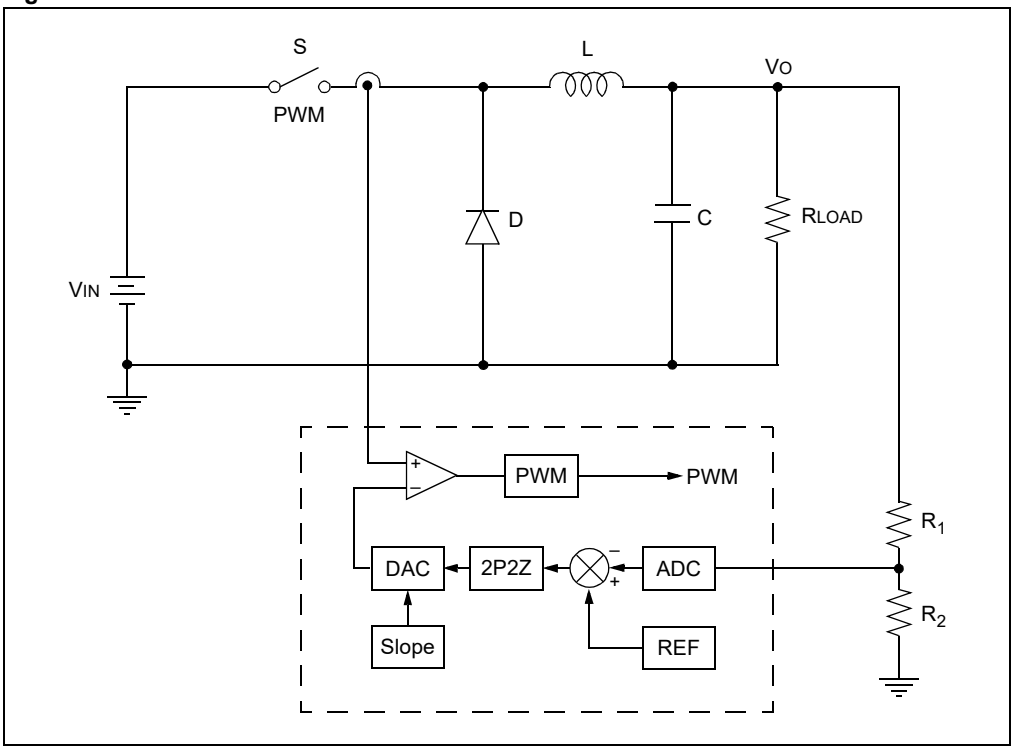
The output of the comparator module can be used in multiple modes at the same time. For example, the comparator output can be used to generate an interrupt, have the ADC take a sample and convert it, and truncate the PWM output, all in response to a voltage being detected beyond its expected value. The SMPS analog comparator module can also be used to wake-up the system from Sleep mode or Idle mode when the analog input voltage exceeds the programmed threshold voltage. The slope compensation module allows the user to utilize built-in hardware-based slope compensation in SMPS applications. The potential applications of the comparator module are numerous and varied.

The following section describes typical applications of the comparator module in power conversion circuits.

## 5.1 Peak Current-Mode Control

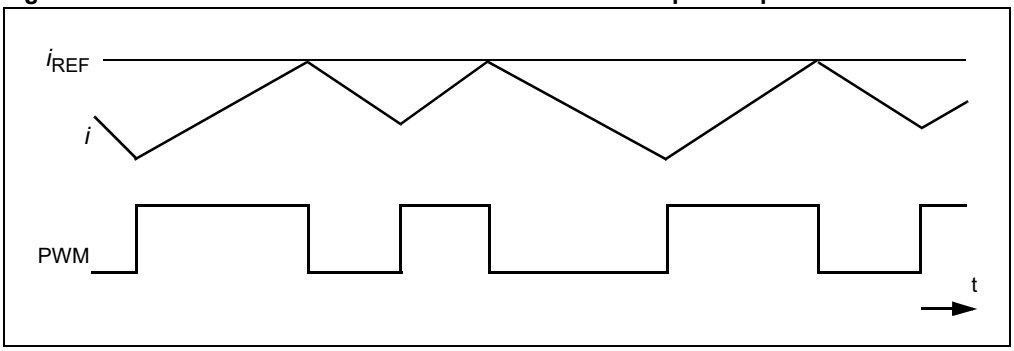
The SMPS topologies, such as Buck, Boost and Buck-Boost, generate subharmonic oscillations when controlled with Peak Current-mode control. These oscillations occur under specific conditions, such as Continuous Current-mode and a duty cycle greater than 50%. The subharmonic oscillations can be damped by using slope compensation. The analog comparator module can be utilized for such applications, eliminating the need for additional external analog circuitry to perform slope compensation. The comparator module is used in conjunction with the PWM module to generate the Current-mode PWM signal. A typical Peak Current Buck mode power supply is illustrated in Figure 5-1.

**Figure 5-1: Buck Converter with Peak Current-Mode Control**



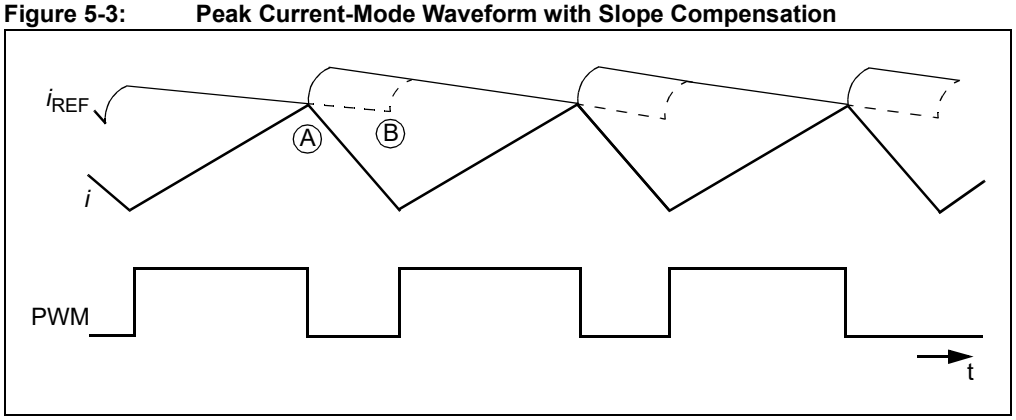

The analog comparator module is configured to reset the PWM module when the measured inductor current peak reaches the current level determined by the outer control loop. The outer control loop consists of the output voltage, measured by the ADC, and compared with a desired voltage reference. The error counts generated are treated with a compensator gain to arrive at the peak current level for the current PWM cycle. The peak current level is applied to the DAC to generate an equivalent analog signal with which the actual inductor current is compared by the comparator. The waveforms of the Peak Current-mode control are as shown in Figure 5-2. Note that the pulse width is different in the consecutive cycles, even though the current reference, $i_{REF}$, is constant.

**Figure 5-2: Peak Current-Mode Waveform without Slope Compensation**



The slope compensation module alters the DAC output voltage slope, hence the reference to the inner current loop. In the absence of the slope compensation module, the output of the DAC is held constant for a given PWM cycle (as shown in Figure 5-2). The slope generation module causes the reference current to slope based on the values set in the register. The slope direction can be set to positive or negative depending on the applications, although negative slope is generally used. The rate of the slope is determined by the SLPxDAT register. The register, DACxDATH, holds the DAC value at the start of the PWM cycle and the DAC value at the end of the PWM cycle is held by the DACxDATL register. The waveforms of the Peak Current-mode control with slope compensation are as shown in Figure 5-3. Note that the pulse width is the same in all cycles for a constant current reference, $i_{REF}$.

**Figure 5-3: Peak Current-Mode Waveform with Slope Compensation**




Example 5-1 shows the settings of the analog comparator module for generating the slope compensated waveforms. Refer to the specific device data sheet for clocking options and trigger assignments. The buck converter in this design operates at an input of 5V and an output of 3.3V, 1A. The operating frequency of the converter is 200 kHz. The period timer for the PWM is set at 200 kHz and the duty cycle is set at 95%. The clock frequency for the DAC module is set at 500 MHz. The current measurement is connected to the positive input of the comparator. The DAC provides the reference current for the peak current trip and is connected internally to the negative input of the comparator. The reference current is generally the output of the compensator (digital filter), which operates on the outer voltage loop error signal. The PWM cycle is terminated when the measured input current exceeds the DAC reference current, $i_{REF}$, as shown by Point A in Figure 5-3. This is due to configuration of the SLPSTOPBx trigger in Figure 5-1.The dashed curve shows the reference current, $i_{REF}$, if SLPSTOPBx is not triggered. In this case, $i_{REF}$ continues until the SLPSTOPAx signal is triggered and is indicated by Point B in Figure 5-3.

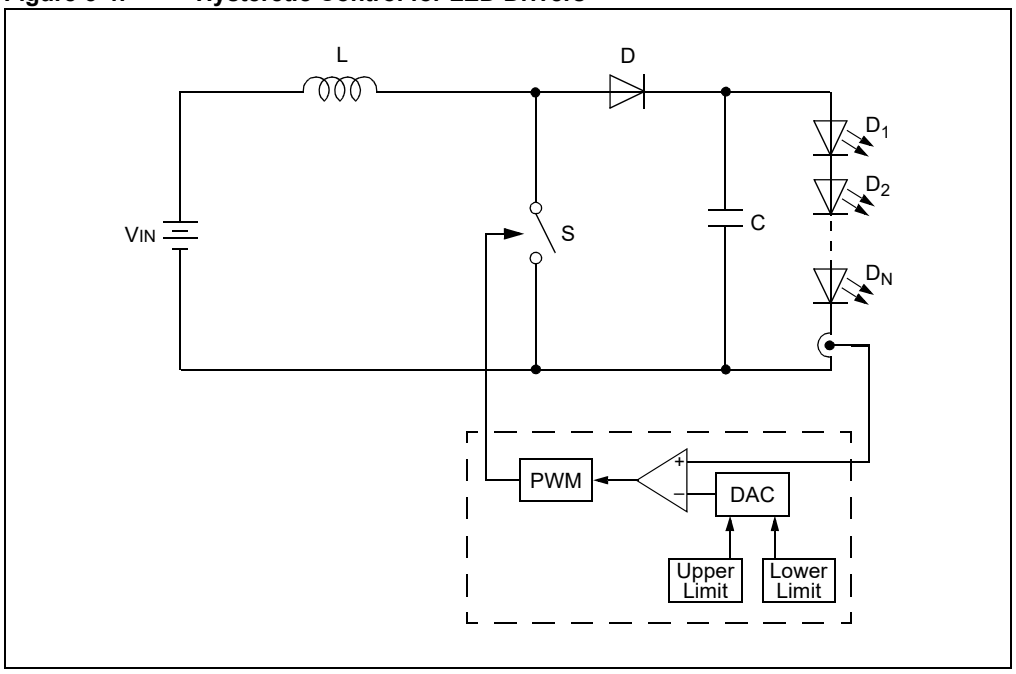
**Example 5-1: Initialize DAC with Slope Compensation**

```
// PWM Configuration
PCLKCONbits.MCLKSEL = 1;          // AFVCO/2 as clock source (500 Mhz)
PG1CONLbits.CLKSEL = 1;           // Clock selected by MCLKSEL
PG1PER = 2499;                    // PWM frequency is 200 kHz, 5 uS period
PG1DC = 2375;                     // 95% duty cycle, 4.75 uS on time
PG1IOCONHbits.PENH = 1;           // PWM Generator controls the PWMxH output pin
PG1IOCONHbits.PENL = 1;           // PWM Generator controls the PWMxL output pin
// PWM PCI setup, use CLDAT when comparator 1 trips
PG1CLPCILbits.PSS = 27;           // PCI source is Comparator 1
PG1CLPCILbits.AQSS = 2;           // LEB active as Acceptance Qualifier
PG1CLPCILbits.AQPS = 1;           // Invert Acceptance Qualifier (LEB not active)
PG1CLPCILbits.TERM = 1;           // Auto terminate as Termination Event
PG1CLPCIHbits.ACP = 3;            // Latched PCI Acceptance Criteria
PG1IOCONLbits.CLDAT = 0b01;       // PWM1L = 1 and PWM1H = 0 if CL event is active
PG1LEBHbits.PHR = 1;              // Rising edge of PWMxH triggers the LEB counter
PG1LEBL = 30;                     // 500 nS LEB timer
// PWM to DAC Trigger setup
PG1TRIGA = 750;                   // ADC Trigger 1 at 1.5 uS, used as SLPSTRT
PG1EVTLbits.ADTR1EN1 = 1;         // PGxTRIGA as trigger source for ADC Trigger 1
PG1TRIGB = 2000;                  // ADC Trigger 2 at 4 uS, used as SLPSTOPA
PG1EVTHbits.ADTR2EN2 = 1;         // PGxTRIGB as trigger source for ADC Trigger 2

PG1CONLbits.ON = 1;               // Enable PWM

// DAC Configuration
DACCTRL1Lbits.CLKSEL = 0;         // AFVCO/2 as clock source (500 Mhz)
DACCTRL2Hbits.SSTIME = 0x8A;      // Default value 552 nS @ 500MHz
DACCTRL2Lbits.TMODTIME = 0x55;    // Default value 340 nS @ 500MHz
DAC1DATHbits.DACDATH = 2703;      // 2.17v steady state value
DAC1DATLbits.DACDATL = 1113;      // 0.89v, value at the end slope
SLP1DATbits.SLPDAT = 41;          // Slope = (2703-1113)*16/((4u-1.5u)/4n)
SLP1CONHbits.SLOPEN = 1;          // Enable Slope compensation
SLP1CONLbits.SLPSTRT = 1;         // PWM1 ADC Trigger 1
SLP1CONLbits.SLPSTOPA = 1;        // PWM1 ADC Trigger 2
SLP1CONLbits.SLPSTOPB = 1;        // Comparator 1
DAC1CONHbits.TMCB = 125;          // 125 * 4 nS = 500 nS blanking time
DAC1CONLbits.CBE = 1;             // Enable comparator blanking
DAC1CONLbits.DACOEN = 1;          // Enable DAC output
DAC1CONLbits.DACEN = 1;           // Enable DAC 1
DACCTRL1Lbits.DACON = 1;          // Enable DAC system
```

## 5.2 Hysteretic Control for LED Drivers

The hysteretic control offers the fastest response to the changing parameters, such as voltage or current. The hysteretic control finds wide usage in LED applications, where the current is required to be in a limited range around the average value. The disadvantage of the hysteretic topology is the variable frequency of operation. Figure 5-4 shows an example circuit where the LED current is controlled to an average value with a tolerance decided by the register values.

**Figure 5-4: Hysteretic Control for LED Drivers**



The comparator uses Hysteretic mode for such applications. The Hysteretic mode is controlled by the HME bit in the SLPxCONH register. In order to enable the Hysteretic mode, the HME bit must be set to '1' and the SLOPEN bit is cleared. The upper limit of the hysteretic control is defined by the DACxDATH register, while the lower limit is defined by the DACxDATL register. In Hysteretic mode, the comparator module has a pair of output signals that are available as Peripheral Pin Select (PPS) inputs: PWM_Req_on and PWM_Req_off. These signals can then be mapped to the PWM PCI input for controlling the PWM outputs. The DAC settings for Hysteretic mode are shown in Example 5-2. Refer to the specific device data sheet for clocking options and trigger assignments.

**Example 5-2: DAC Settings for Hysteretic Mode**

```
/* Clock Selection */
PCLKCONbits.MCLKSEL = 3;        // Master Clock Source is APLL
PG1CONLbits.CLKSEL = 1;         // Clock selected by MCLKSEL
while(!_APLLCK)                 // Wait for PLL lock

PG1IOCONHbits.PENH = 1;         // Enable H output
PG1IOCONHbits.PENL = 1;         // Enable L output
PG1IOCONLbits.FFDAT = 0b11;     // FF PCI data is 0b11
// PPS setup
RPINR12bits.PCI8R = 168;        // 'PWM_Req_On' signal from DAC to PCI8
RPINR12bits.PCI9R = 169;        // 'PWM_Req_Off' signal from DAC to PCI9
// FF PCI setup
PG1FFPCILbits.TSYNCDIS = 1;     // Termination of latched PCI occurs immediately
PG1FFPCILbits.TERM = 0b111;     // PCI 9 (PWM_Req_Off)
PG1FFPCILbits.PSS = 8;          // PCI 8 (PWM_Req_On)
PG1FFPCIHbits.ACP = 0b100;      // Latched rising edge
PG1CONLbits.ON = 1;             // Enable PG1

// DAC initialization
DACCTRL1Lbits.CLKSEL = 2;       // APLL
DAC1DATLbits.DACDATL = 0x400;   // Lower cmp limit, 0.825 V
DAC1DATHbits.DACDATH = 0xC00;   // Upper cmp limit, 2.475 V
DAC1CONHbits.TMCB = 100;        // 2/500 MHz * 100 = 400 nS
DAC1CONLbits.CBE = 1;           // Enable comparator blanking
SLP1CONLbits.HCFSEL = 1;        // 1 = PWM1H
SLP1CONHbits.HME = 1;           // Hysteretic Mode
DAC1CONLbits.INSEL = 1;         // CMP1B input
DAC1CONLbits.DACOEN = 1;        // Output DAC voltage to DACOUT1 pin
DAC1CONLbits.DACEN = 1;         // Enable DAC module
DACCTRL1Lbits.DACON = 1;        // Enable DAC1
```

## 5.3 Using DAC as Voltage Reference for External Comparator

If the DAC output is used as a reference voltage for a comparator external to the dsPIC33 device, the Transition mode's transient response can cause unwanted comparator trips when changing DACDAT values. When the DAC is in Transition mode, the blanking feature (CBE = 1) can be set to mask the internal comparator's output. However, this blanking feature is not available on an external comparator.

A work around for this use case is to set the TMODTIME[9:0] bits in the DACCTRL2L register to zero to disable Transition mode. The DAC will slew slower to the new target voltage.

# 6.0 LIMITATIONS

## 6.1 Comparator Input Range

The High-Speed Analog Comparator with Slope Compensation DAC has a limitation for the input Common-Mode Range (CMR) to not exceed ($AV_{DD}$ + 0.2V). This means that the input to the comparator (the selected CMPx input pin) should be within this range. As long as the input is within the CMR, the comparator output will be correct. Any input exceeding the CMR limitation will cause the comparator input to be saturated.

## 6.2 PMD DAC Output Range

The DAC is implemented using a digital Pulse Density Modulation (PDM) scheme and a multi-stage RC output filter. Operation near minimum or maximum values results in bit stream patterns that incur higher noise on the filtered output. Noise and spikes at DAC output degrade performance capabilities, such as offset and INL. The performance specifications listed in the device data sheet electrical specifications are only valid within the 5% to 95% range.

## 7.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the High-Speed Analog Comparator with Slope Compensation DAC are:

| Title | Application Note # |
|---|---|
| No related application notes at this time. | N/A |

**Note:** Please visit the Microchip website (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 families of devices.

## 8.0 REVISION HISTORY

### Revision A (July 2016)

This is the initial version of this document.

### Revision B (June 2018)

Changes device family name to dsPIC33/PIC24.

Removes the Advance Information watermark from the footer.

### Revision C (October 2019)

Updates **Section 1.0 "Introduction"**, **Section 3.0 "Control Registers"**, **Section 4.1 "Comparator Stage"**, **Section 4.1.1 "Comparator Inputs"**, **Section 4.2 "Pulse Density Modulation (PDM) DAC"**, **Section 4.2.1.1 "Slope Generation Mode"**, **Section 4.2.1.2 "Hysteretic Mode"**, **Section 4.3 "Operation in Sleep and Idle Mode"**, **Section 5.1 "Peak Current-Mode Control"** and **Section 5.2 "Hysteretic Control for LED Drivers"**.

Adds **Section 4.1.2 "Comparator Outputs"**, **Section 4.1.3 "Comparator Interrupt"** and **Section 5.3 "Using DAC as Voltage Reference for External Comparator"**.

Adds Equation 4-1.

Updates Figure 2-1 and Table 3-1.

Updates Example 4-4, Example 5-1 and Example 5-2.

Updates Register 3-1, Register 3-4, Register 3-5, Register 3-6, Register 3-7, Register 3-9 and Register 3-10.

Updates the document title from High-Speed Analog Comparator Module to High-Speed Analog Comparator with Slope Compensation DAC.

Minor grammatical and formatting changes throughout the document.

### Revision D (January 2021)

Minor edits throughout document.

### Revision E (January 2021)

Updates **Section 1.0 "Introduction"** and **Section 4.2.1.1 "Slope Generation Mode"**.

Updates Figure 2-1 and Figure 4-2.

Updates Register 3-6 and Register 3-7.

Updates Example 4-4 and Example 5-2.

### Revision F (June 2021)

Updates Register 3-6 and Register 3-7.

Updates **Section 4.2 "Pulse Density Modulation (PDM) DAC"**.

Updates Equation 4-1.

Updates Example 4-3.

Adds **Section 6.2 "PMD DAC Output Range"**.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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